



Programmable Delay Circuit for Sparker Signal Analysis

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Abstract

The sparker echo signal had been recorded along with the EPC recorder trigger on audio cassettes in a dual channel analog recorder. The sparker signal in the analog form had to be digitised for further signal processing techniques to be performed on it to classify the seafloor sediment properties. A specific purpose oriented programmable delay circuit was developed to generate the necessary delay so that the A/D conversion could start just before the arrival of the echo from the water bottom interface.

Introduction

An EG & G sparker system was operated during the cruise of RV GAVESHANI [1]. The sparker return signal and the trigger signal from the EPC recorder were stored on a dual channel analog tape recorder. It was desired to perform mathematical functions viz. determination of the probability density function of the echo peak and echo integration on the sparker signal to determine the characteristics of the sea floor sediment. In order to carry out the above signal processing techniques, the sparker echo signal had to be digitised. The depth of operation of the sparker survey was approximately 60 metres and hence the time duration between the EPC trigger and the echo from the water bottom interface was roughly 80 ms. A circuit was designed to generate a programmable delay so that the digitisation of the signal could commence just before the arrival of the bottom echo. The circuit incorporates analog and CMOS ICs.

Description of the Digitisation System

As shown in Fig. 1, the echo signal was fed to a PCL 718 high performance data acquisition card installed in the PC/AT. The A/D conversion was performed in the external pulse trigger mode whereby the conversion would begin only on the arrival of the external pulse. This external trigger pulse was generated by the delay circuit electronics.

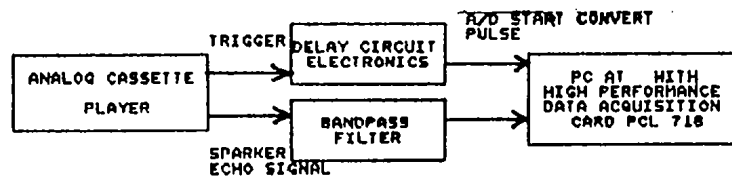


Fig. 1

Details of the Delay Circuit Electronics

LM 393 Comparator

A schematic diagram of the circuit is shown in Fig. 2. The EPC trigger consists of a short burst of five pulses of frequency 1.117 kHz and maximum amplitude (V_{max}) of 0.9 volts as shown in Fig. 3. The EPC trigger is fed to the non inverting input while a reference voltage V_{ref} of 0.8 volts from a dc power supply is applied to the inverting input of the comparator op amp LM 393A

[2]. When the trigger input exceeds the reference voltage, the comparator produces an output pulse of approximately 0.7 msec duration which is fed to the master reset input pin of the CMOS programmable timer CD 4541B.

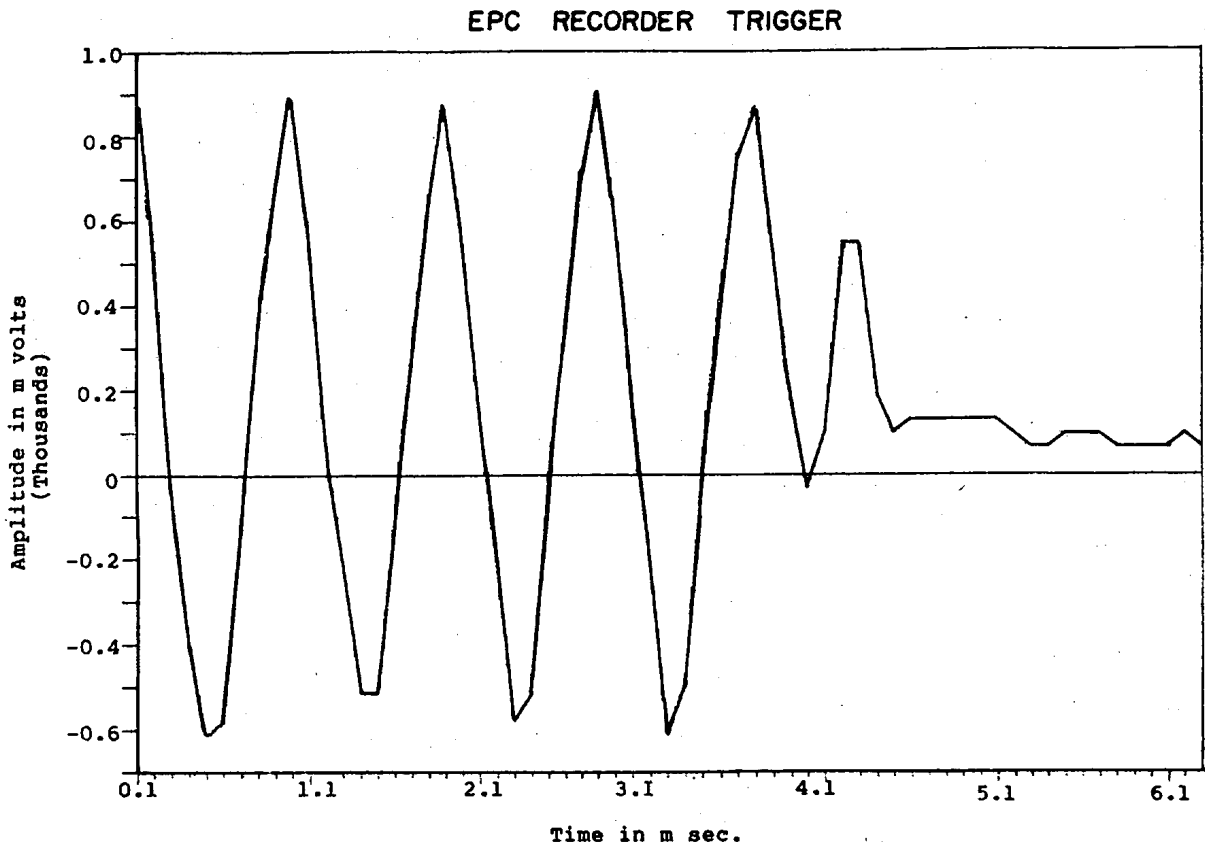
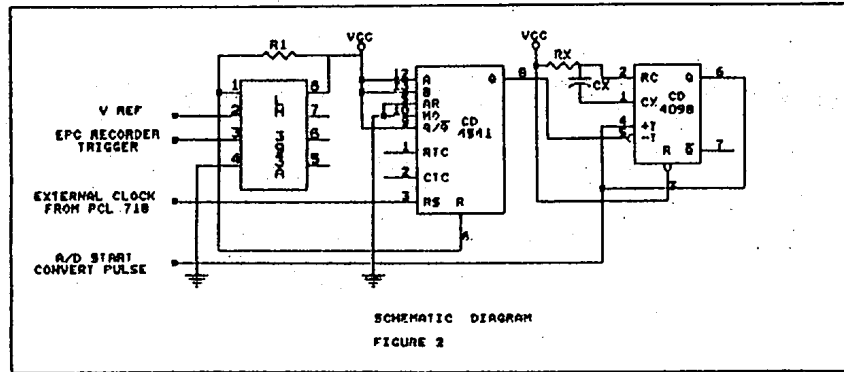


Fig. 3

Programmable Timer CD 4541B

The CD 4541B [3] is a programmable timer whose output changes state after 2^{N-1} counts where N can be chosen for different configurations of pin 12(A) and pin 13 (B). The possible values of N available were 8, 10, 13 and 16. For a desired delay of t msec the time required to count 2^{N-1} counts should equal to t msec. When N is high, the number of counts increases and hence the clock frequency of the counter increases thereby increasing the accuracy of the delay period. Hence N was chosen to be 16 for which pins A and B were tied to VDD. Hence the output changes state after 2^{15} (32768) counts. The external clock is chosen from the PCL 718 card which has a clock output whose frequency is programmable through software. The output pulse changes state from high to low whereas the A/D start convert pulse should be a rising pulse. Hence the output of CD4541B is fed to the input of a dual monostable multivibrator CD 4098B.

Monostable Multivibrator 4098B

The monostable is used in the falling edge trigger mode and hence produces an output pulse as soon as the CD4098B [3] output changes state from high to low. The output pulse duration is determined by the values of the timing capacitor C_x and resistor R_x where $T_x = 1/2 R_x C_x$. In the circuit R_x is 12K and C_x is 220 nF for which T_x is 1.32 msec., which is substantial to be a good start convert pulse.

Programming the Frequency of the External Clock Input to CD 4541B

The waveform of a typical sparker signal echo obtained from a survey at 60 m depth is shown in Fig.4. For an 8 kjoules sparker operation the duration of the transmitted pulse is 10 ms from point A to B as shown in Fig 4. The first bottom echo return starts at point D which is approximately 80 ms from point A. Between C and D, the signal amplitude is fairly low nearing zero. On power up of the digitisation process, the clock output of the PCL 718 is programmed such that the delay duration is equal to the duration of the transmitted pulse and the digitisation process starts at point B. A certain algorithm senses the duration C to D where the signal level is practically zero and then waits for the echo signal to cross a certain predetermined value at point E. The time duration between point B and E is computed through a knowledge of the sampling frequency and the number of values digitised between B and E. The new output clock frequency of PCL718 is then calculated through a program so that the start of A/D conversion shifts from point B to B' which is 10 msec before point E. For every successive echo, the duration between the point B' and E is calculated and the new clock frequency determined so that the sampling begins 10 ms before the predetermined value at point E.

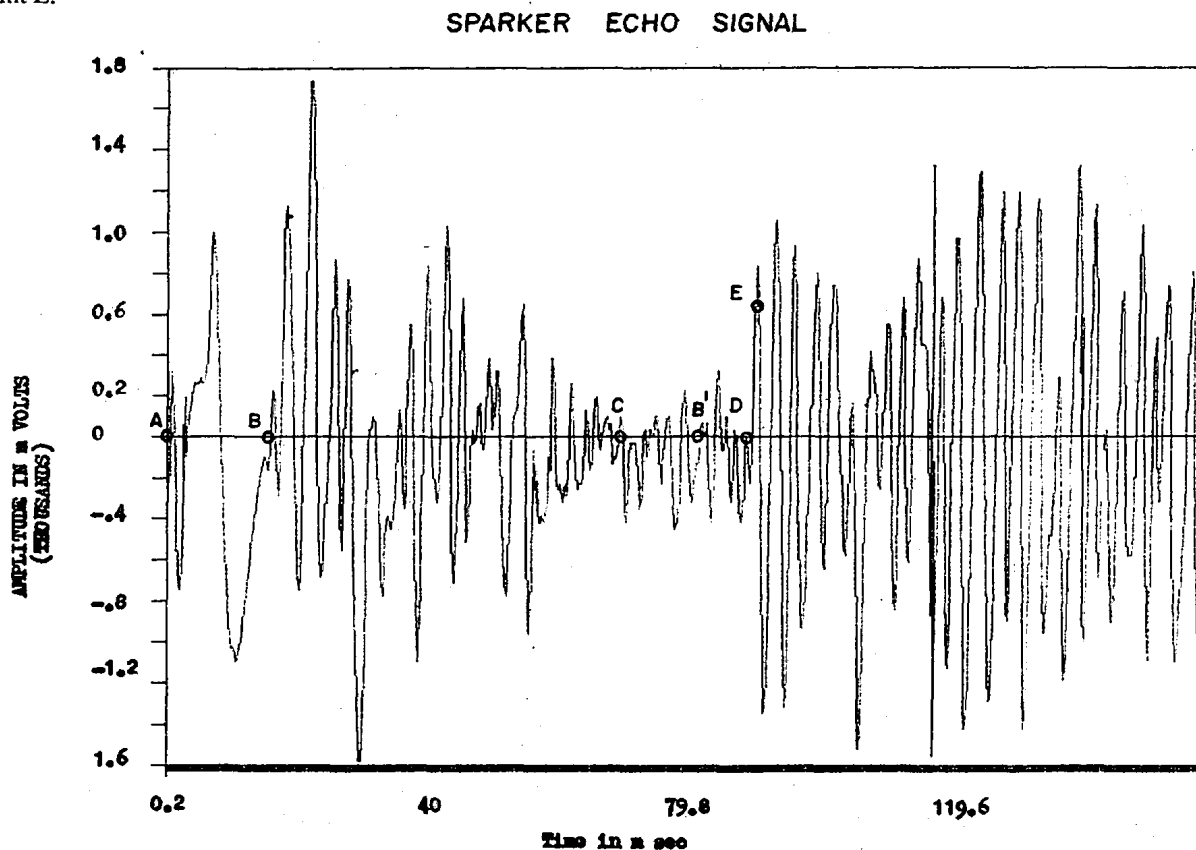


Fig. 4

Application

The programmable delay circuit has successfully aided in analysing the sparker signal and determining the probability density function of the peak echo amplitude and also perform echo integration. Since the peak value detection was performed through a program, it was necessary that the part of the waveform from point A to B' in Fig. 4 be deleted from digitisation, as in some cases, the echo peak value was less than the peak of the signal between A and B'. Additionally, it prevented the digitisation of redundant data since only the bottom echo return signal was of interest for carrying out the seabed studies.

Conclusion

Since the design requirement was a typical and for a specific purpose, it was developed in the laboratory with the available components, the PCL718 card and the PC/AT to carry out post processing on the sparker signal. A future programme incorporates the design of a real time echo processor in which the delay circuit can be used.

Acknowledgements

I wish to thank Shri R. R. Nair, Project leader, PMN for his encouragement in carrying out the work. I also wish to thank Dr. B. N. Desai, Director, N. I. O. for allowing me to use the laboratory facilities in performing this work. Thanks are also due to Shri T. Sudhakar and V. Khedekar for their help in plotting waveforms and the circuit diagram.

References

- [1] Technical Report on Oceanographic Cruise of RV GAVESHANI (Cruise 144), A National Institute of Oceanography Internal Publication.
- [2] Linear Databook, National Semiconductor Corporation
- [3] RCA Solid State Databook, CMOS Integrated Circuits.